CLAIMS

1. A semiconductor memory device comprising:

a bit line;

a memory cell coupled to the bit line; and

a word line coupled to the memory cell,

wherein a first time between receiving a write command for a write operation in order to write data to the memory cell and beginning the write operation is different from a second time between receiving a refresh command for a refresh operation in order to refresh data stored in the memory cell and beginning the write operation.

2. The device according to claim 1, wherein the refresh operation is started after the write operation.

3. The device according to claim 1, wherein the write operation is a delayed write operation.

4. The device according to claim 1, wherein the write operation includes activation of the word line.

5. The device according to claim 1, wherein the write operation is executed by a plurality of clock cycles.

6. The device according to claim 1, wherein the write operation is completed in a write cycle time from activating the word line to deactivating the word line and precharging the bit line.

7. The device according to claim 1, wherein a third time between receiving a read command for a read operation in order to read data from the memory cell and beginning the read operation is different from the first time.

8. The device according to claim 7, wherein the refresh operation is started after the write operation.

9. The device according to claim 8, wherein the write operation is a delayed write operation.

10. A semiconductor memory device comprising:

a bit line;

a memory cell coupled to the bit line;

a word line coupled to the memory cell;

an input data register which stores data to be written the memory cell,

wherein a first time between receiving a write command for a write operation in order to write data stored in the input data register to the memory cell and beginning the write operation is different from a second time between receiving a refresh command for a refresh operation in order to refresh data stored in the memory cell and beginning the write operation.

11. The device according to claim 10, wherein the refresh operation is started after the write operation.

12. The device according to claim 10, wherein the write operation is a delayed write operation.

13. The device according to claim 10, wherein the write operation includes activation of the word line.

14. The device according to claim 10, wherein the write operation is executed by a plurality of clock cycles.

15. The device according to claim 10, wherein the write operation is completed in a write cycle time from activating the word line to deactivating the word line and precharging the bit line.

16. The device according to claim 10, wherein a third time between receiving a read command for a read operation in order to read data from the memory cell and beginning the read operation is different from the first time.

17. The device according to claim 16, wherein the refresh operation is started after the write operation.

18. The device according to claim 16, wherein the write operation is a delayed write operation.